REMARKS

Claims 1-21 are pending in the present application. Claim 7 is identified as allowable but is objected to by the Office. Claims 1-6, and 8-21 have been rejected.

Allowable Claim(s)

Claim 7 is acknowledged by the Office as being allowable, but is objected to for depending from a rejected base claim. In consideration of the arguments herein, regarding the rejected base claim, withdrawal of the objection of claim 7 is requested.

Rejections under § 112

In sections 2 and 3 of the Office Action, the Examiner rejected claims 5-6, 15, and 17 under 35 U.S.C. § 112. The rejections are hereby traversed.

Claims 5-6

While it is believed original claim 5 was proper, in the interest of furthering prosecution, Claim 5 has been amended to better clarify the invention. The scope of claim 5 has not been changed. Claim 6 was rejected for depending from a rejected claim. Withdrawal of the rejection of claims 5 and 6 under § 112 is respectfully requested.

Claim 15

The Office states that claim 15, when read in context, is not understood. Applicants assert that claim 15 as written is definite and particularly points and distinctly claims the subject matter as required by § 112. To assist the Office in better understanding claim 15, specific

elements of a particular embodiment disclosed in the figures will be correlated to claimed elements. The correlation of claim 15 elements to figure elements is not meant to limit the scope of claim 15.

Claim 15 recites a set of address nodes (A[n:2] of element 101) to provide address data for address location A(n) through A(2), such address data would be received at address bit locations ADDR[n:2] of element 230 of FIG. 4 or element 236 of FIG. 6.

Claim 15 further recites a first output node (A[x] of element 101) to provide one of an address data for address location A(1) and a data lane enable signal based upon a mode of operation. In FIG. 4, during a first mode of operation, NODE A[x] of element 101 provides address data to the node of element 230 labeled WRITE_ENB(UPPER_MID). This data, when asserted, is an enable signal to select a specific 8 bits of the DATA[31:0]. In FIG. 6, during a second mode of operation, the same node A[x] acts to provide an address data bit such as would be received at address bit location A(1) of element 236 of FIG.6. The recited second output node of claim 15 corresponds to node A[w] of element 101, which can provide a lane enable signal to WRITE_ENB(UPPER) or an address data bit to address bit location A(0). The third output node of claim 15 corresponds to node A[y] of element 101, where it can provide a lane enable signal to WRITE_END(LOWER_MID) in the mode illustrated in FIG. 4, or act to expand the memory space by providing an address data bit to address location A[n+1] of element 236 of FIG. 6. The dual functionality of the first, second and third nodes of claim 15 based on the mode of operation, is believed to be particularly pointed out and distinctly claimed in claim 15. Withdrawal of the rejection of claim 15 is respectfully requested.

Claim 17

Claim 17 has been amended to remove the word "wherein," and to insert the words "further comprising." This change is believed to overcome the Office's rejection of claim 17. Withdrawal of the rejection of claim 17 is respectfully requested.

Rejections under § 102

Claim 1, 19

In sections 4 and 5 of the Office Action, the Examiner rejected claim 1under 35 U.S.C. § 102 (e) as being anticipated by Chang (2003/0005247 A1). The rejection is hereby traversed.

The Office has rejected claim 1 stating:

> Regarding Claims 1, 10, 16, 19, and 21, Chang teaches a memory access system in which a first mode of operation is used to access a first addressing range ("first portion of memory storage location") and a second mode of operation is used to access a second addressing range ("second portion of memory storage location"). It is understood that "data lane" enable information is simply any signal that can be used to indicate what portion of data is to be accessed. Therefore, any signal being used by the system of Chang to access the various addressing ranges can in fact be a data lane signal (See page 4, claim 1); in addition, it is understood that memory address bits are used in the facilitation of access to a particular memory location.

The Applicants respectfully disagree.

It is recognized at MPEP section 2121, that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). In addition, the identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

Claim 1 recites:

> A method comprising the steps of:
> when in a first mode of operation, utilizing a first output to provide a first data lane enable for facilitating access of a portion of a first memory storage location associated with a first memory address; and
> when in a second mode of operation, utilizing the first output to provide an address bit of a second memory address for facilitating designation of a second memory storage location.

The Office has not shown the identical invention of claim 1 as required. Chang does not disclose a first output that is utilized in the first and second modes of operation as recited. In the first mode, the first output facilitates accessing a portion of a first memory storage location identified by a first memory address. In the second mode, the first output provides part of the second memory address. Note, in the first mode the first output does not provide any portion of a memory address as in the second mode. The only text referenced by the Office is that of Chang's claim 1, which does not disclose the two modes of operation, nor does it disclose utilizing a first output to provide a first data lane enable for facilitating access of a portion of a first memory storage location associated with a first memory address.

For at least the reason(s) indicated, each and every element of claim 1 is not disclosed by Chang. Therefore, withdrawal of the rejection under § 102 of claim 1, and rejections of claims dependent upon claim 1, is respectfully requested, and their allowance solicited. In addition, those claims depending from claim 1 disclose additional non-obvious subject matter.

Claim 19 discloses similar limitations to claim 1 in a system claim, and is allowable at least for reasons analogous to those made with respect to claim 1. Therefore withdrawal of the rejection under § 102 of claim 19, and rejections of claims dependent upon claim 19, is respectfully requested, and their allowance solicited. In addition, those claims depending from claim 19 disclose additional non-obvious subject matter.

Claim 21 discloses similar limitations to claim 1 in another method claim, and is allowable at least for reasons analogous to those made with respect to claim 1. Therefore withdrawal of the rejection under § 102 of claim 21, and rejections of claims dependent upon

claim 21, is respectfully requested, and their allowance solicited. In addition, those claims depending from claim 21 disclose additional non-obvious subject matter.

Claim 16

In sections 4 and 5 of the Office Action, the Examiner rejected claim 16 under 35 U.S.C. § 102 (e) as being anticipated by Chang (2003/0005247 A1).

Claim 16 recites:

> An apparatus comprising:
> a first register having an output to indicate one of a first mode of operation and a second mode of operation;
> an address control portion having an input coupled to the output of the first register, and an output to indicate a value of an address bit when in the first mode of operation;
> a first data lane enable control portion having an input coupled to the output of the first register, and an output to indicate a first data lane enable value when in the second mode of operation; and
> an output pin coupled to the output of the address control portion and the output of the first data lane enable control portion. (Emphasis Added)

The Office has not identified in Chang an address control portion as recited, nor has the Office disclosed a first data lane enable control portion. More specifically, Chang does not disclosed an output pin coupled to the output of an address control portion and the output of a first data lane enable control portion as recited.

For at least the reason(s) indicated, each and every element of claim 16 is not disclosed by Chang. Therefore withdrawal of the rejection under § 102 of claim 16, and rejections of claims dependent upon claim 1, is respectfully requested, and their allowance solicited. In addition, those claims depending from claim 16 disclose additional non-obvious subject matter.

Those claims rejected under § 103 depend from allowable base claims. Withdrawal of the rejections under § 103 is respectfully requested.

Applicant(s) does not believe that any additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 50-2469.

If, for any reason, the Office is unable to allow the Application on the next Office Action, and believes a telephone interview would be helpful, the Examiner is respectfully requested to contact the undersigned attorney or agent.

Respectfully submitted,

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Date

J. Gustav Larson, Reg. No. 39,263
Attorney for Applicant(s)
TOLER, LARSON & ABEL, L.L.P.
P.O. Box 29567
Austin, Texas 78755-9567
(512) 327-5515 (phone)
(512) 327-5452 (fax)